



NEWS RELEASE

Forte Releases Latest Version of Cynthesizer SystemC High-Level Synthesis

Adds SystemC 2.2 Support, Automated Design Partitioning/Interface Creation, Enhanced Scalability Improvements

SAN JOSE, CALIF. — June 29, 2009 — Forte Design Systems (www.ForteDS.com), a leading provider of High-Level Synthesis software, today began volume shipments of the latest version of Cynthesizer™, SystemC synthesis software for hardware and electronic system level (ESL) design.

Anchoring this version of Cynthesizer are several new features, including SystemC 2.2 support, tools for partitioning complex hierarchical systems, automated generation of complex interfaces, enhanced control-based design support, memory support upgrades and scalability improvements.

“Solutions based on ANSI-C are inherently limited in their ability to model complex concurrent hardware architectures including interfaces, control and datapath blocks,” remarks Sean Dart, Forte’s president and chief executive officer. “Cynthesizer includes new automated interface generation and design partitioning that leverages the modeling power of SystemC to move it further ahead in the breadth of designs styles covered and quality of results achieved.”

Fast, Accurate Design and Verification with Forte Cynthesizer

Cynthesizer lets designers choose either SystemC 2.1v1 or the latest SystemC 2.2 IEEE standard. Forte supports SystemC because designs modeled behaviorally in SystemC are faster than register transfer level (RTL) simulations and more accurate than ANSI-C based models. Further, SystemC provides a standardized means of representing critical hardware concepts not available in pure ANSI-C solutions such as concurrency, bit accuracy, timing and hierarchy. Together with Cynthesizer, designs can be accurately modeled and verified using behavioral simulations and synthesized directly from that representation without the need for manual work once the RTL code is created.

Design Partitioning and Interface Generation

The existence of a wide variety of advanced, complex, validated and highly customizable interface intellectual property (IP) blocks enhances engineering productivity when designing complex hierarchical and multi-block systems. Cynthesizer adds an interface IP generator for design teams to customize validated, synthesizable interfaces for use in their designs. These interfaces range from standard streaming or buffer interfaces to complex interfaces, such as line buffers often used in imaging designs.

Cynthesizer also includes automated design partitioning for behavioral design specifications expressed serially to be quickly and easily split into multiple parallel blocks. Its partitioning feature divides the design into multiple parts while automatically determining data dependency

between blocks and creating an appropriate interface. This enhanced process streamlines the design exploration and creation process by utilizing pre-verified interface templates reducing overall time and risk.

Finally, Cynthesizer now offers transaction logging through an integration with Springsoft's Verdi™ Automated Debug System. This capability enables designers to log complex transactions for memories or over interfaces directly to Springsoft's Fast Signal Database (FSDB).

Forte will demonstrate Cynthesizer in Booth #1225 at the 46th Design Automation Conference (DAC) that will take place July 26-31 at the Moscone Center in San Francisco. To schedule a private demonstration of Cynthesizer, go to www.ForteDS.com/DAC2009. For details about DAC, visit: www.dac.com.

Pricing and Availability

Cynthesizer comes standard with Forte's transaction level modeling (TLM) synthesis capability, with U.S. pricing starting at \$275,000. Cynthesizer's Partitioning and Interface Generator features start at \$40,000 (U.S.) as an add-on to Cynthesizer to further improve productivity.

About Forte Design Systems

Forte Design Systems is a leading provider of software products that enable design at a higher level of abstraction. Its innovative high-level synthesis technology allows design teams creating complex electronic systems from algorithmic designs using ASICs, FPGAs, and SoCs to significantly reduce their overall design and verification time. Forte is headquartered at 100 Century Center Court, San Jose, Calif. 95112. For more information, visit www.ForteDS.com.

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