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Thursday, May, 6th 2010

News Analysis

Forte acquires Arithmatica

By Bill Murray

09/28/09

Forte Design Systems, provider of SystemC-driven high level synthesis (HLS) tools, today announced that it has acquired Arithmatica, a provider of RTL-to-gate datapath synthesis tools and intellectual property (IP).

Arithmatica claims that its CellMath Designer datapath synthesis tool and its CellMath IP reduce area and power, and improve performance in datapath-intensive designs. The tool works with common logic synthesis tools and utilizes existing RTL code, synthesis scripts and technology libraries. Forte will integrate the Arithmatica synthesis technology into its HLS tool, Cynthesizer, to improve the tool's quality of results (QoR), and also maintain the Arithmatica technology as stand-alone products. The first integrated product is expected to be available around the end of 2009.

The acquisition also adds CellMath's floating point, integer and application IP to Forte's IP library. The CellMath library contains optimized floating point architectures, configurable for bit widths, rounding modes, and precision. The library also contains multi-function parts that can produce floating point functions using shared resources to reduce the combined area.

Integrated Datapath Synthesis

Forte's Cynthesizer HLS tool already synthesizes RTL for both control- and datapath-intensive designs from a single description source. The description uses standard SystemC without proprietary language extensions. Brett Cline, Forte's vice president of marketing and sales, said "Users target critical parts of the design for datapath synthesis to enhance QoR by our datapath synthesizer. Now, with this acquisition, Cynthesizer can also import custom datapath components designed with CellMath Designer. The integrated toolset will automatically identify functionality that would benefit from custom datapath synthesis. The result? Cynthesizer will produce smaller, faster RTL designs."

Cline continued "Cynthesizer does all of the synthesis from the high level SystemC description. The datapath elements either parts designated by the user or complex part opportunities found by the tool are put through CellMath Designer. In this flow, designers can leverage the datapath synthesis tool to generate smaller and faster parts, which Cynthesizer can use. This nearly always produces a better overall design." However, embedded datapath synthesis is not a requirement. "It is something that users can turn on during HLS to get better results," said Cline.

Does CellMath Designer have a separate set of constraints or is there a single set for both "pieces of technology?" How are these constraints written, given that Cynthesizer uses SystemC and CellMath Designer doesn't? Cline replied "Constraints and the actual part function are passed from Cynthesizer to CellMath Designer during runtime, using a language and commands similar to those used by CellMath Designer stand-alone. This process is automatic and invisible to the designer." He continued "The user can designate a section of code for which a custom datapath part is desired and use a directive to instruct Cynthesizer to have that part built. The designer can also use a command line switch to instruct Cynthesizer to globally seek opportunities to improve QoR."

QoR and Upstream Insight

How big is the QoR enhancement delivered by the integrated tools? Cline said "The integration work is still in progress. However, some of our early prototyping shows area reductions of greater than 10 percent. We don't have specific quantification of performance and power, yet. However, I would just point out that CellMath Designer has algorithms that specifically optimize power for datapath parts, while Cynthesizer's previous internal datapath synthesis does not."

Forte claims that the integrated approach provides better upstream insight into the downstream implementation flow. How? According to Cline, there are two issues. "First, like Cynthesizer, CellMath Designer knows how the part looks in a specific technology library and clock speed. So, it has a very accurate estimate of how that part will perform after logic synthesis. Its ability to accurately estimate and build a high-quality part is superior to that of the existing Cynthesizer datapath synthesis engine. Second, users who have deployed CellMath Designer standalone will eventually be able to leverage the legacy IP RTL in the HLS flow. So, Cynthesizer will be able to import and utilize the part in its schedule, just as if it had itself used CellMath Designer to build the part. This means that users can not only increase their IP ROI, but also work "offline" on critical datapath elements. That's what delivers the insight."

Ease of Use

What changes for the Cynthesizer user? Cline said "In the HLS flow, users do exactly what they have always done with Cynthesizer. There are absolutely no changes to their input or use model. Cynthesizer explores the general architecture of the design and, when it finds interesting parts that are not already in its library, it will run CellMath Designer to generate an accurate estimate of that part. Cynthesizer will use that information to build the schedule."

Cline continued "It's worth noting that, unlike some HLS tools, Cynthesizer does not need a library of parts built with a logic synthesis tool ahead of HLS. This eliminates the days of effort often required to pre-build a library for each technology and speed. However, some users build a characterized library of parts as a starting point. But, since you cannot pre-build every possible part, Cynthesizer can use CellMath Designer to augment the pre-built library during synthesis – something that, again, many other HLS tools cannot do."

Cline said "This acquisition affords designers three entry points into the Forte design environment – our established SystemC-driven HLS route, and now via RTL design and IP-based design." See figure 1.

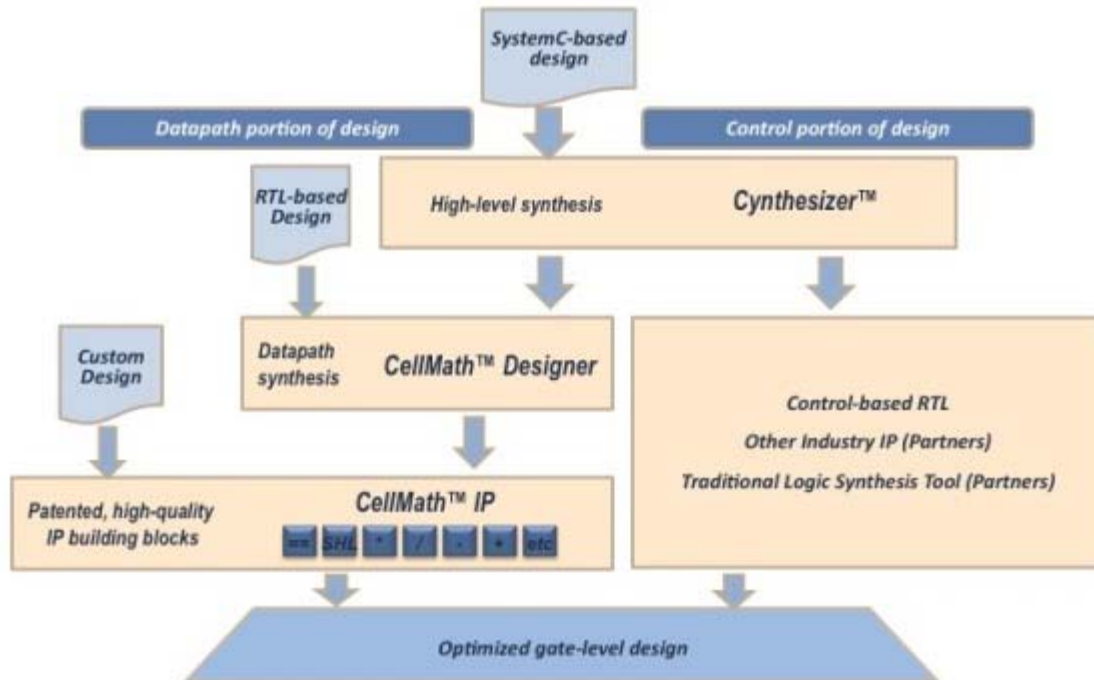


Figure 1: The Arithmatica acquisition expands the entry points to the Cynthesizer environment (Source: Forte Design Systems)

"For example, Fujitsu Microelectronics Europe uses high-level SystemC which calls the Cynthesizer's datapath synthesis tool to get the best QoR for that portion of the design," said Cline. He continued "Imagination Technologies and Digital Media Professionals both use CellMath Designer as a standalone RTL-driven datapath synthesis tool; and Xilinx uses CellMath IP in its Virtex parts, without Forte tools."

Installed Base

What is Arithmatica's installed base in terms of seats/IP licenses? Cline said "We are not making that specific information public. However, I will say that the OEM agreement with Imagination Technologies gives us a pretty wide reach into the market. We believe we have about 650 worldwide users of the combined Forte and Arithmatica tools today."

Further Reading:

[Forte boosts Cynthesizer's automation capabilities](#). Bill Murray. SCDsource, August 2009.

ESL Design and Verification by B. Bailey, G. Martin and A. Piziali. Morgan Kaufmann, 2007. [Chapter 11: Hardware Implementation](#).

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